IEEE Xplore RELEASE 2.1

Search Result - Print Format

< Back to Previous Page

Key: **IEEE JNL** = IEEE Journal or Magazine, **IEE JNL** = IEE Journal or Magazine, **IEEE CNF** = IEEE Conference, **IEE CNF** = IEE Conference, **IEEE STD** = IEEE Standard

1. **A transparent online memory test for simultaneous detection of functional faults and soft errors in memories**
   Thaller, K.; Steininger, A.;
   Reliability, IEEE Transactions on
   Volume 52, Issue 4, Dec. 2003 Page(s):413 - 422
   IEEE JNL

2. **A highly-efficient transparent online memory test**
   Thaller, K.;
   Test Conference, 2001. Proceedings. International
   30 Oct.-1 Nov. 2001 Page(s):230 - 239
   IEEE CNF

3. **Predicting the number of fatal soft errors in Los Alamos national laboratory's ASC Q supercomputer**
   Michalak, S.E.; Harris, K.W.; Hengartner, N.W.; Takala, B.E.; Wender, S.A.;
   Device and Materials Reliability, IEEE Transactions on
   Volume 5, Issue 3, Sept. 2005 Page(s):329 - 335
   IEEE JNL

Indexed by Inspec®

Key: IEEE JNL = IEEE Journal or Magazine, IEE JNL = IEE Journal or Magazine, IEEE CNF = IEEE Conference, IEE CNF = IEE Conference, IEEE STD = IEEE Standard

1. **A highly-efficient transparent online memory test**
   Thaller, K.;
   Test Conference, 2001. Proceedings. International
   30 Oct.-1 Nov. 2001 Page(s):230 - 239
   IEEE CNF

2. **Achieving fault secureness in parity prediction arithmetic operators: general conditions and implementations**
   Nicolaidis, M.; Manich, S.; Figueras, J.;
   European Design and Test Conference, 1996. ED&TC 96. Proceedings
   11-14 March 1996 Page(s):186 - 193
   IEEE CNF

3. **On the testing of microprogrammed processor**
   Hwang, S.; Rajsuman, R.; Malaiya, Y.K.;
   Microprogramming and Microarchitecture. Micro 23. Proceedings of the 23rd Annual Workshop and Symposium., Workshop on
   27-29 Nov. 1990 Page(s):260 - 266
   IEEE CNF

4. **ECC-on-SIMM test challenges**
   Dell, T.J.;
   Test Conference, 1994. Proceedings., International
   2-6 Oct. 1994 Page(s):511 - 515
   IEEE CNF

5. **Circuit techniques for a VLSI memory**
   Mano, T.; Yamada, J.; Inoue, J.; Nakajima, S.;
   Solid-State Circuits, IEEE Journal of
   Volume 18, Issue 5, Oct 1983 Page(s):463 - 470
   IEEE JNL

6. **Design of self-checking sequential machines**
   Dhawan, S.; De Vries, R.C.;
   Computers, IEEE Transactions on
   Volume 37, Issue 10, Oct. 1988 Page(s):1280 - 1284
   IEEE JNL

7. **An organization and interface for sensor-driven semiconductor process control systems**
   Najafi, N.; Wise, K.D.;
   Semiconductor Manufacturing, IEEE Transactions on
   Volume 3, Issue 4, Nov. 1990 Page(s):230 - 238
   IEEE JNL

8. **Fault-secure parity prediction Booth multipliers**
   Nicolaidis, M.; Duarte, R.O.;
   Design & Test of Computers, IEEE
   Volume 16, Issue 3, July-Sept. 1999 Page(s):90 - 101
   IEEE JNL

9. **Fast and compact error correcting scheme for reliable multilevel flash memories**
   Rossi, D.; Metra, C.; Ricco, B.;
   On-Line Testing Workshop, 2002. Proceedings of the Eighth IEEE International

8-10 July 2002 Page(s):221 - 225

IEEE CNF

10. **Fast and compact error correcting scheme for reliable multilevel flash memories**
Rossi, D.; Metra, C.; Ricco, B.;
Memory Technology, Design and Testing, 2002. (MTDT 2002). Proceedings of the 2002 IEEE International Workshop on
10-12 July 2002 Page(s):27 - 31

IEEE CNF

11. **Redundant optical storage system using DVD-RAM library**
Tanabe, T.; Takayanagi, M.; Tatemiti, H.; Ura, T.; Yamamoto, M.;
Mass Storage Systems, 1999. 16th IEEE Symposium on
15-18 March 1999 Page(s):80 - 87

IEEE CNF

12. **Flip chip MCM-L using known good die**
Hodges, D.; Adamjee, W.; Corona, C.; Czarnowski, J.M.; Eklund, R.; Guajardo, J.; Youngblood, A.;
Multichip Modules and High Density Packaging, 1998. Proceedings. 1998 7th International Conference on
15-17 April 1998 Page(s):358 - 361

IEEE CNF

13. **A unified on-line and off-line BIST scheme for ROMs**
Yeung, D.; Sun, X.; Olson, M.;
Communications, Computers, and Signal Processing, 1995. Proceedings. IEEE Pacific Rim Conference on
17-19 May 1995 Page(s):469 - 472

IEEE CNF

14. **VLSI implementation of a self-checking self-exercising memory system**
Rennels, D.A.; Kim, H.;
Fault-Tolerant Computing, 1991. FTCS-21. Digest of Papers., Twenty-First International Symposium
25-27 June 1991 Page(s):170 - 177

IEEE CNF

15. **A built-in Hamming code ECC circuit for DRAMs**
Furutani, K.; Arimoto, K.; Miyamoto, H.; Kobayashi, T.; Yasuda, K.; Mashiko, K.;
Solid-State Circuits, IEEE Journal of
Volume 24, Issue 1, Feb. 1989 Page(s):50 - 56

IEEE JNL

16. **Testing check bits at no cost in RAMs with on-chip ECC**
Ramanathan, P.; Saluja, K.K.; Franklin, M.;
Computers and Digital Techniques, IEE Proceedings-
Volume 140, Issue 6, Nov 1993 Page(s):304 - 312

IEE JNL

17. **System-on-chip oriented fault-tolerant sequential systems implementation methodology**
Pontarelli, S.; Cardarilli, G.C.; Malvoni, A.; Ottavi, M.; Re, M.; Salsano, A.;
Defect and Fault Tolerance in VLSI Systems, 2001. Proceedings. 2001 IEEE International Symposium on
24-26 Oct. 2001 Page(s):455 - 460

IEEE CNF

18. **Upset-tolerant CMOS SRAM using current monitoring: prototype and test experiments**
Calin, T.; Vargas, F.L.; Nicolaidis, M.;
Test Conference, 1995. Proceedings., International
21-25 Oct. 1995 Page(s):45 - 53

IEEE CNF

19. **Zero cost testing of check bits in RAMs with on-chip ECC**
Ramanathan, P.; Saluja, K.K.; Franklin, M.;
VLSI Test Symposium, 1992. '10th Anniversary. Design, Test and Application: ASICs and Systems-on-a-Chip', Digest

of Papers., 1992 IEEE
7-9 April 1992 Page(s):292 - 297
IEEE CNF